UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,587	09/29/2003	Theodore Doros	42P16636	9936

7590 06/07/2006

Jan Carol Little
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,587	DOROS ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *23-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed on March 20, 2006. Claims 1-25 are pending, in which claims 23-25 are non-elected without traverse.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman (5,976,769) taken with Blatchford, JR. et al (2002/0187434).

Chapman teaches a method comprising: forming a layer material (208,206 in Figs 2a-2c; on a silicon wafer 202 (Fig 2a, col 2, lines 46-65;), the silicon wafer 202 having variations in surface topology comprising at least one thick region and at least one thin region, the layer 208,206 of material having variations in surface topology comprising at least one thick regions and at least one thin region corresponding to the thick regions and the thin regions of the wafer 202, respectively; forming at least one narrow region (e.g. 217 in Figs 2g,3) and at least one wide region (e.g. 218 in Fig 2g,3) in the layer of material (Figs 2c-2g,3), the narrow regions and the wide regions corresponding to the thick regions and the thin regions of the wafer, respectively (Figs 2g,3; col 2, line 66 through col 3). Re claim 2, exposing photoresist photosensitive resin 210 (Fig 2a) disposed on the layer 208,206 of material to light through a mask having a pattern to which near-resolution marks have been added so that a first photoresist pattern 212 having larger resolution and a smaller near-resolution photoresist pattern 211 having a width W are formed thereon (Figs 2c-3; col 2, line 66 through col 3); and removing portions of the layer of material 208,206 to leave the narrow regions and the wide regions. Re claim 3, wherein the method comprises characterizing the thick regions of the wafer as first zones (Fig 2a-2g,3); characterizing the thin regions of the wafer as second zones; and forming the narrow regions in the first zones and the wide regions in the second zones (Figs 2g,3). Re claim 4, wherein the method comprises setting first imaging compensation for the first zones and second imaging compensation for the second zones (Figs 2c-2g; col 2, line 45 through col 3); and removing areas of the layer of material to leave the narrow regions in the first zones and the wide regions in the second zones.

Chapman already teaches a lithographic process for forming a semiconductor device as a microelectronic system device, but lacks mentioning the process for forming a micro-electro-mechanical system (MEMS) device.

However, Blatchford teaches (at paragraph 0009; Figs 1A-3; paragraphs 0008,18-25) that a lithographic process are used in forming devices including microelectronic integrated semiconductor devices, optical devices and micro-electro-mechanical system (MEMS) devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the lithographic process of forming at least one narrow region and at least one wide region in the layer of material, the narrow regions and the wide regions corresponding to the thick regions and the thin regions of the silicon wafer, respectively, of Chapman, in forming devices including micro-electro-mechanical system (MEMS) devices, microelectronic integrated semiconductor devices, optical devices, as taught by Blatchford. This is because of the desirability to employ the lithographic process for forming the micro-electro-mechanical system (MEMS) devices having a small size of fine pattern features.

2. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al (6,387,808) taken with Blatchford, JR. et al (2002/0187434).

Schiltz teaches a method comprising: forming a layer 16/20 material on a silicon wafer 10(Fig 2a,col 2, lines 33-67; Fig 5a, col 5, line 5-67), the silicon wafer 10 having variations in surface topology comprising at least one thick region and at least one thin region, the layer 20/16 of material having variations in surface topology comprising at least one thick regions and at least one thin region corresponding to the thick regions and the thin regions of the wafer 10, respectively; forming at least one narrow region and at least one wide region in the layer 20/16 of material, the narrow regions (narrow region 21 in Fig 2b; and 202 in Fig 5b) and the wide regions (wider region 21 in Fig 2b; and wider region 204 in Fig 5b) corresponding to the thick regions and the thin regions of the wafer 10, respectively; and exposing photoresist photosensitive resin 20 disposed on the layer 16 of material to light through a mask 22 (Fig 2a; col 2, lines 41-47; line 64 through col 3; col 3, lines 41-50) having a pattern to which near-resolution marks have been added, wherein a plurality of openings 24 are formed between the added near-resolution masks; and removing portions of the layer 16/20 of material to leave the

narrow regions and the wide regions (narrow region 21 in Fig 2b; and 202 in Fig 5b; and wider region 21 in Fig 2b; and wider region 204 in Fig 5b). Re claim 2, further comprising of exposing photoresist photosensitive resin 20 disposed on the layer 16 of material to light through a mask 22 (Fig 2a; col 2, lines 41-47; line 64 through col 3; col 3, lines 41-50) having a pattern to which near-resolution marks have been added, wherein a plurality of openings 24 are formed between the added near-resolution masks; and removing portions of the layer 16/20 of material to leave the narrow regions and the wide regions (narrow region 21 in Fig 2b; and 202 in Fig 5b; and wider region 21 in Fig 2b; and wider region 204 in Fig 5b); and removing portions of the layer 16/20 of material to leave the narrow regions and the wide regions (narrow region 21 in Fig 2b; and 202 in Fig 5b; and wider region 21 in Fig 2b; and wider region 204 in Fig 5b). Re claim 3, wherein the method comprises characterizing the thick regions of the wafer as first zones; characterizing the thin regions of the wafer as second zones; and forming the narrow regions in the first zones and the wide regions in the second zones (col 2, lines 20-25; col 5, lines 1-25; Figs 1; 2a-2c;5a-5c). Re claim 4, wherein the method comprises setting first imaging compensation for the first zones and second imaging compensation for the second zones (col 1, lines 26-33; Figs 1; 2a-2c;5a-5c; col 2, lines 20-25; col 5, lines 1-25); and removing areas of the layer 16/20 of material to leave the narrow regions in the first zones and the wide regions in the second zones (narrow region 21 in Fig 2b; and 202 in Fig 5b; and wider region 21 in Fig 2b; and wider region 204 in Fig 5b).

Schiltz already teaches a lithographic process for forming a semiconductor device as a microelectronic system device, but lacks mentioning the process for forming a micro-electro-mechanical system (MEMS) device.

However, Blatchford teaches (at paragraph 0009; Figs 1A-3; paragraphs 0008,18-25) that a lithographic process are used in forming devices including microelectronic integrated semiconductor devices, optical devices and micro-electro-mechanical system (MEMS) devices.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the lithographic process of forming at least one narrow region and at least one wide region in the layer of material, the narrow regions and the wide regions corresponding to the thick regions and the thin regions of the silicon wafer, respectively, of Schiltz, in forming devices including micro-electro-mechanical system (MEMS) devices,

microelectronic integrated semiconductor devices, optical devices, as taught by Blatchford. This is because of the desirability to employ the lithographic process for forming the micro-electro-mechanical system (MEMS) devices having a small size of fine pattern features.

Claim Rejections - 35 USC § 103

3. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Schiltz et al (6,387,808) or Chapman (5,976,769) taken with Ledger (5,502,564).

Schiltz teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography, and wherein the method comprises forming at least one narrow region and at least one wide region in the layer 20/16 of material, the narrow regions (narrow region 21 in Fig 2b; and 202 in Fig 5b) and the wide regions (wider region 21 in Fig 2b; and wider region 204 in Fig 5b) corresponding to the thick regions and the thin regions of the wafer 10, respectively. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

Re claim 5, Schiltz or Chapman lacks mapping to determine the thick and thin regions. Re claim 6, wherein the mapping is ellipsometric, laser, or capacitance.

However, Ledger teaches determining and measuring variation of wafer thickness by mapping the substrate surface (col 1, lines 7-10; col 10, lines 18-32; col 7, lines 30-31; Figs 1-8), wherein the mapping techniques includes ellipsometric mapping (at Fig 1; col 7, lines 60-63; col 8, lines 1-4), laser mapping (col 8, lines 26-29); and capacitance mapping (col 1, lines 56-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to carry out the method of Schiltz or Chapman to determine the thick and thin regions by mapping the substrate surface, wherein techniques for mapping includes ellipsometric, laser, or capacitance, as taught by Ledger. This is because of the desirability to precisely determine the locations of thick and thin regions on the wafer so that narrow and wide regions can be correspondingly and precisely formed respectively thereon.

4. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al (6,387,808) or Chapman (5,976,769) taken with Kozhukh (6,437,903).

Schiltz teaches a method as applied above to claims 1-4, and fully incorporated herein. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

Schiltz or Chapman thus lacks mentioning a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods of claims 1-4 above.

However, Kozhukh teaches (at col 6, lines 58-61; col 4, lines 10-45) about employing a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the methods of Schiltz or Chapman in a machine-accessible medium, as taught by Kozhukh so that when accessed by a machine, cause the machine to perform the stored methods in an automatic manner.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al or Chapman (6,387,808), taken with Kozhukh (6,437,903), as applied to claims 7-10, and further of Ledger (5,502,564).

Schiltz and Kozhukh teaches a method as applied to claims 7-10 above, wherein Kozhukh teaches (at col 6, lines 58-61; col 4, lines 10-45) about employing a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods, and wherein Schiltz teaches an unevenness of substrate topography and a method comprises forming at least one narrow region and at least one wide region in the layer 20/16 of material, the narrow regions (narrow region 21 in Fig 2b; and 202 in Fig 5b) and the wide regions (wider region 21 in Fig 2b; and wider region 204 in Fig 5b) corresponding to the thick regions and the thin regions of the wafer 10, respectively. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

Re claim 11, the references including Schiltz or Chapman lack mapping to determine the thick and thin regions.

However, Ledger teaches determining and measuring variation of wafer thickness by mapping the substrate surface (col 1, lines 7-10; col 10, lines 18-32; col 7, lines 30-31; Figs 1-8),

wherein the mapping techniques includes ellipsometric mapping (at Fig 1; col 7, lines 60-63; col 8, lines 1-4), laser mapping (col 8, lines 26-29); and capacitance mapping (col 1, lines 56-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to carry out the method of Schiltz or Chapman to determine the thick and thin regions by mapping the substrate surface, as taught by Ledger. This is because of the desirability to precisely determine the locations of thick and thin regions on the wafer so that narrow and wide regions can be correspondingly and precisely formed respectively thereon.

6. Claims 12,13,16,17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al (6,387,808) or Chapman (5,976,769) taken with Van Der Plas (5,015,602) and Atkinson (5,155,053).

Schiltz teaches a method comprising: forming a layer 16/20 material on a silicon wafer 10(Fig 2a,col 2, lines 33-67; Fig 5a, col 5, line 5-67), the silicon wafer 10 having variations in surface topology comprising at least one thick region and at least one thin region, the layer 20/16 of material having variations in surface topology comprising at least one thick regions and at least one thin region corresponding to the thick regions and the thin regions of the wafer 10, respectively; and forming at least one narrow region and at least one wide region in the layer 20/16 of material, the narrow regions (narrow region 21 in Fig 2b; and 202 in Fig 5b) and the wide regions (wider region 21 in Fig 2b; and wider region 204 in Fig 5b) corresponding to the thick regions and the thin regions of the wafer 10, respectively, wherein the method includes exposing photoresist photosensitive resin 20 disposed on the layer 16 of material to light through a mask 22 (Fig 2a; col 2, lines 41-47; line 64 through col 3; col 3, lines 41-50) having a pattern to which near-resolution marks have been added, wherein a plurality of openings 24 are formed between the added near-resolution masks; and removing portions of the layer 16/20 of material to leave the narrow regions and the wide regions (narrow region 21 in Fig 2b; and 202 in Fig 5b; and wider region 21 in Fig 2b; and wider region 204 in Fig 5b). Re claim 16, wherein the method comprises characterizing the thick regions of the wafer as first zones; characterizing the thin regions of the wafer as second zones; and forming the narrow regions in the first zones and the wide regions in the second zones (col 2, lines 20-25; col 5, lines 1-25; Figs 1; 2a-2c;5a-5c). Re claim 17, wherein the method comprises setting first imaging compensation for the

first zones and second imaging compensation for the second zones (col 1, lines 26-33; Figs 1; 2a-2c;5a-5c; col 2, lines 20-25; col 5, lines 1-25); and removing areas of the layer 16/20 of material to leave the narrow regions in the first zones and the wide regions in the second zones (narrow region 21 in Fig 2b; and 202 in Fig 5b; and wider region 21 in Fig 2b; and wider region 204 in Fig 5b). Chapman also teaches a method as applied above to claims 1-4, and fully incorporated herein, wherein there is an unevenness of substrate topography.

Re claim 12, Schiltz or Chapman lacks forming a sacrificial layer on the first layer, and lacks using direct write of a pattern on photoresist. Re further claim13, wherein direct writing uses electron beam, ultraviolet light, x-rays, or optical beam.

However, Van Der Plas teach (at Figs 9-11) forming a plurality of layers on the silicon wafer, wherein the plurality of layers includes a sacrificial layer 15 formed on a first layer 20/18, and wherein the sacrificial layer has a variations in surface topology comprising a thick and thin regions corresponding to the thick and thin regions of the first layer 18/20, respectively. Atkinson teaches (at Figs 19-22; col 9, lines 17-30) to form a pattern having small and near-resolution limit by direct writing on a photoresist 60, wherein, re further claim 13, the direct writing uses electron beam, ultraviolet light, x-rays, or optical beam (col 9, lines 17-25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device structure of Schiltz or Chapman by forming a plurality of layers on the silicon wafers, wherein the plurality of layers includes a sacrificial layer formed on a first layer, as taught by Van Der Plas. This is because of the desirability to form an etch stop layer on the first layer so that the layer can be etched in an selective manner. Additionally, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form a pattern in the first layer of Schiltz by direct writing on a photoresist layer formed on the first layer, as taught by Atkinson, in which the direct writing uses electron beam, ultraviolet light, x-rays, or optical beam (col 9, lines 17-25). This is because of the desirability to form a small and near-resolution pattern on the silicon wafer, wherein processing steps and cost are reduced since it is directly written on the photoresist by directly irradiating electron beam, ultraviolet light, x-rays, or optical beam, without using a photomask.

7. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al (6,387,808) or Chapman (5,976,769) taken with Van Der Plas (5,015,602) and Atkinson (5,155,053), as applied to claims 12,16,17 above, and further of Banks et al (5,112,440).

The references including Schiltz, Van Der Plas, and Atkinson teaches a method as applied to claims 12,16 and 17 above. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

The combined references teach a photoresist, but lack mentioning a photosensitive polymer (claim 14) or a non-polymer photoresist (claim 15).

However, Banks teaches (at col 5, lines 19-21) patterning a layer by using a photoresist material, wherein the photoresist includes conventional photosensitive and non-photosensitive polymers.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the pattern of the references including Schiltz or Chapman by employing a photoresist material including conventional photosensitive and non-photosensitive polymers, as taught by Banks. This is because photosensitive and non-photosensitive polymers are alternative and art recognized equivalent materials for forming a photoresist so that small and near-resolution pattern can be effectively formed.

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al (6,387,808) or Chapman (5,976,769), taken with Van Der Plas (5,015,602) and Atkinson (5,155,053), as applied to claims 12,13,16,17 above, and further of Ledger (5,502,564).

The references including Schiltz, Van Der Plas, and Atkinson teach a method as applied to claims 12,13, 16 and 17 above, wherein Schiltz teaches an unevenness of substrate topography and a method comprises forming at least one narrow region and at least one wide region in the layer 20/16 of material, the narrow regions (narrow region 21 in Fig 2b; and 202 in Fig 5b) and the wide regions (wider region 21 in Fig 2b; and wider region 204 in Fig 5b) corresponding to the thick regions and the thin regions of the wafer 10, respectively. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

Re claim 18, the references including Schiltz or Chapman lack determining the thick and thin regions by mapping the substrate surface.

However, Ledger teaches determining and measuring variation of wafer thickness by mapping the substrate surface (col 1, lines 7-10; col 10, lines 18-32; col 7, lines 30-31; Figs 1-8), wherein the mapping techniques includes ellipsometric mapping (at Fig 1; col 7, lines 60-63; col 8, lines 1-4), laser mapping (col 8, lines 26-29); and capacitance mapping (col 1, lines 56-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to carry out the method of the references including Schiltz or Chapman to determine the thick and thin regions by mapping the substrate surface, as taught by Ledger. This is because of the desirability to precisely determine the locations of thick and thin regions on the wafer so that narrow and wide regions can be correspondingly and precisely formed respectively thereon.

9. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz et al (6,387,808) or Chapman (5,976,769), taken with Van Der Plas (5,015,602) and Atkinson (5,155,053), as applied to claims 12,13,16 and 17 above, and further of Kozhukh (6,437,903).

The references including Schiltz, Van Der Plas, and Atkinson teach a method as applied to claims 12,13,16 and 17 above. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

The relied references thus lack mentioning a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods.

However, Kozhukh teaches (at col 6, lines 58-61; col 4, lines 10-45) about employing a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the methods of the references including Schiltz or Chapman in a machine-accessible medium, as taught by Kozhukh so that when accessed by a machine, cause the machine to perform the stored methods in an automatic manner.

10. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schiltz (6,387,808) or Chapman (5,976,769), taken with Van Der Plas (5,015,602), Atkinson (5,155,053), and Banks (5,112,440), as applied to claims 14-15 above, and further of Kozhukh (6,437,903).

The relied references including Schiltz, Van Der Plas, Atkinson, and Banks teach a method as applied to claims 14-15 above. Chapman also teaches a method as applied above to claims 1-4, wherein there is an unevenness of substrate topography.

The relied references thus lack mentioning a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods.

However, Kozhukh teaches (at col 6, lines 58-61; col 4, lines 10-45) about employing a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the methods.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the methods of the references including Schiltz or Chapman in a machine-accessible medium, as taught by Kozhukh so that when accessed by a machine, cause the machine to perform the stored methods in an automatic manner.

Response to Amendment

11. Applicant's amendment and remarks filed March 20, 2006 with respect to pending claims have been considered, but they are not persuasive and moot in view of the new ground(s) of rejection.

** Applicant's mainly remarked that Schiltz or Chapman does not address "...***micro-electrical-mechanical system (MEMS) device***...", but is limited to ***semiconductor devices***...".

In response, Blatchford clearly teaches (at paragraph 0009; Figs 1A-3; paragraphs 0008,18-25) the lithographic process used in forming devices including *integrated devices (i.e. semiconductor microelectronic device),* optical devices *and micro-electro-mechanical system (MEMS) devices.*

Applicants appears to allege that "...fabrication of a micro-electrical- mechanical system (MEMS) device, such as a vibrator, whose surface is not planar but includes fingers of a sort,

each of which includes a weight (i.e., length-height-width). The weights of the fingers should be uniform...".

In response, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978). Indeed, nowhere in the claims mention the above limitations.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-17

Michael Trinh
Primary Examiner